Application No.: 09/496,516 SAR-12165A
Amendment dated: July 9, 2003
Reply to Office Action of: April 9, 2003

Remarks/Arguments:

The pending claims are 15-24. Claims 20 and 21 have been amended. No new matter has been introduced therein.

The disclosure has been objected to because of typographical errors. Since the required changes have been made, applicants request that the objection be withdrawn.

The Abstract has been objected to. Since a new Abstract has been provided, applicants request that this objection be withdrawn.

Applicants gratefully acknowledge the indication in the Office Action that claims 22-24 have been allowed.

Claim 20 has been objected to. This ground for objection is overcome by amending claim 20 to depend from claim 19. Because the third data value is not defined in claim 19, the phrase "a third data value" is not improper in claim 20. As no prior art has been cited against claim 20, it is now in condition for allowance.

Claim 21 has also been amended to correct an inadvertent error. No new matter is added by this amendment.

Claims 15, 17-19 and 21 have been rejected under 35 U.S.C. § 103(a) as unpatentable over Sekigawa et al. (U.S. Patent No. 4,606,050) in view of Nimishakavi (U.S. Patent No. 5,594,763). The rejection is respectfully traversed.

Claim 15 recites, in part

> data means for producing a third data value when the count value is equal to or greater than a first threshold value and a fourth data value when the count value is equal to or less than a second threshold value; and
>
> signal generating means for producing a second signal including the third data value and the fourth data value.

The Office Action acknowledges that Sekigawa et al. "does not teach two predetermined values in determining a second signal comprising a high and low logic or third and fourth data value." To make up for this deficiency in Sekigawa et al., the Office Action contends that Nimishikavi teaches the feature. The Office Action contends that Nimishakavi teaches the above recitations. Relying upon col. 5, lines 7-15, the Office Action contends that Nimishakavi "teaches that when a counter reaches a first predetermined value one output pulse is sent. And when a second predetermined value is reached, a different output pulse is sent." Even with this recitation, the combination of Sekigawa et al. and Nimishikavi do not meet the limitations of claim 15. Furthermore, there can be no suggestion to combine Sekigawa et al. and Nimishikavi because Nimishikavi teaches away from the combination and because the only suggestion to combine the references comes from Applicants' own disclosure.

As described in the Office Action, Sekigawa et al. discloses counting circuit that includes an up-down counter which "counts up or counts down counting clock pulses according to the level of signal HS." The output signal of the counter is compared to an initialization value. If, at the end of the bit time, the counter output is greater than the initialization value, the comparator produces an "H" value. If the counter output is less than the initialization value, the comparator produces an "L" value. (See col. 3, line 54 through col. 4, line 2). As indicated in the Office Action, Sekigawa et al. do not disclose or suggest using two threshold values to produce the second signal.

Although Nimishakavi teaches two different output pulses being sent, it does not teach generating third and fourth count values in response to different respective threshold values in a way that meets the limitations of claim 15. In particular, claim 15 requires:

> data means for producing a third data value when the count value is equal to or greater than a first threshold value and a fourth data value when the count value is equal to or less than a second threshold value

Specifically, Nimishakavi discloses a down-counter that produces a first output pulse when the count equals a first predetermined value (e.g., 16) and that a second output pulse is generated with the count equals a second predetermined value (e.g. 0). (col. 5, lines 7-15). These output pulses are generated by counter 40 (col. 5, lines 9, 11-12; Figure 4). Claim 15, however, requires that the "data means" produce "a third data value when the count value is equal to or greater than a first threshold value and a fourth data value when the count value is

equal to or less than a second threshold value." In Nimishakavi, pulses are produced when the count value equals predetermined values. This differs from the subject invention in two ways. First, Nimishakavi produces pulses, not data values. Second, in Nimishakavi, pulses are produced only when the count value equals the predetermined values, not when it is greater than or equal to one value and less than or equal to the other value, as required by the claim. Since Nimishakavi does not teach what the Office Action contends, combining it with Sekigawa et al. would not produce applicants' invention, even if there were some basis to attempt to make the combination.

Furthermore, it would not be obvious to combine the two devices because they are directed to different devices and operate differently. Sekigawa et al. is directed to a system for detecting and recovering a transmitted signal. Nimishikavi, on the other hand, is directed to a digital phase-locked loop. The purpose of Nimishakavi is merely to produce an oscillatory signal that tracks frequency and phase variations exhibited by edges of an input signal. As such, Nimishakavi requires pulse signals to be produced by the down counter. If levels were produced, as taught by Sekigawa et al., the Nimishakavi circuit would not work; the receive clock generator, to which the pulses are provided, operates on pulse signals, not on levels. (See col. 5, lines 7-15). Thus, the function of Nimishakavi would be defeated by the combination.

Furthermore, in Sekigawa et al., counter 31 is an up-down counter that counts up or counts down. Specifically, "it counts up when the level of signal HS is `H', and it counts down when the level of signal HS is `L'." (col. 3, lines 62-66). Nimishakavi, on the other hand, views up/down counters as prior art and obsolete, in view of its invention. (col. 1, lines 34-39). "Instead of the up/down counters used in the prior art" Nimishakavi uses "an N-bit down counter 40 in order to determine when the clock transitions in a receive clock are to be made." (col. 4, lines 6-9). Accordingly, Nimishakavi teaches away from the device of Sekigawa et al.' and teaches away from applicants' device. Because it teaches away from the deivce of Sekigawa et al., it would not have been obvious to combine the two devices.

The first and second threshold values provide an advantage to the subject invention that is not found in either Sekigawa et al. nor Nimishakavi. In particular, these threshold values add

hysteresis to the integrator, making the integrator less sensitive to high frequency noise. (See the subject specification at page 16, line 20 through page 17, line 3.

For the above reasons, claim 15 is not subject to rejection under 35 U.S.C. § 103(a) as unpatentable over Sekigawa et al. in view of Nimishakavi. Claims 17-18 depend from claim 15. Therefore, they are also not subject to the same rejection for at least the same reasons that claim 15 is not subject to rejection.

Claim 19 recites, in part, "clock synchronization means for producing a clock synchronization signal." The Office Action acknowledges that Sekigawa et al. does not teach this feature. It contends, nevertheless, that Nimishakavi teaches it. Relying on col. 5, lines 12-34, the Office Action contends that Nimishakavi produces "a clock synchronization signal (RxDPLL Out) when the count value is equal to or greater than a first threshold value or predetermined value." Applicants respectfully disagree with this contention.

On occasion, the system in Nimishakavi may need to be synchronized because "it may occur" that a data bit is too wide. When that happens and the counter has counted down to zero without detecting an edge, counter 40 is reset to the start count value 31. "Re-synchronization occurs very quickly" when the next edge is detected. (col. 5, lines 25-26) (emphasis added). That is, a pulse is generated that resets the counter to count value 31. The resetting allows the counter to renew its downward counting while the system seeks the next edge. The pulse itself does not cause synchronization. The pulse simply gives the remainder of the system more time to synchronize itself. More specifically, "[r]e-synchronization occurs. . .when the next edge is finally detected by the edge detector 46." (col. 5, lines 25-27). Furthermore, claim 19 requires that the clock synchronization means produce the clock synchronization signal when the count value is equal to or greater than the first threshold value. Nimishakavi, however, teaches only that the counter is reset if the counter reaches a value of zero and no edge has been detected. Because Nimishakavi uses a down-counter, the analogy to the present invention would be the counter reaching a value less than zero. This is impossible, however, because the Nimishakavi counter counts only from 31 to zero.

Also, in Nimishakavi, the counter itself is reset when the count value of zero is reached. This is not the same as the subject invention. In the subject invention, the synchronization

signal synchronizes the clock signal that is applied to the counter, not just the counter output value. Accordingly, Nimishakavi does not produce a clock synchronization signal as recited in claim 19.

In addition, Nimishikavi teaches away from the Sekigawa et al. device and from applicants' device, as discussed above with respect to claim 15.

Accordingly, for all of the above reasons, claim 19 is not subject to rejection under 35 U.S.C. §103(a) as unpatentable over Sekigawa et al. in view of Nimishakavi. Since claims 20 and 21 depend from claim 19, they too, are not subject to the same rejection for at least the same reasons that claim 19 is not subject to rejection.

Claim 16 has been rejected under 35 U.S.C. § 103(a) as unpatentable over Sekigawa et al. in view of Nimishakavi and further in view of Lu (U.S. Patent No. 5,652,773). The rejection is traversed. Claim 16 depends from claim 15. As shown above, claim 15 is not subject to rejection under 35 U.S.C. § 103(a) as unpatentable over Sekigawa et al, in view of Nimishakavi.

Lu concerns a digital phase locked loop for data separation. Lu also does not disclose or suggest the data means of claim 15 of the subject application. In particular, the output value of the up/down counter 42 of Lu is not compared to any threshold value. Instead, it is used to adjust a predicted phase value (see col. 5, lines 31-60). Accordingly, because Lu does not provide the material that is missing from Sekigawa et al. and Nimishakavi, claim 15 is not subject to rejection over Sekigawa et al., Nimishakavi and Lu and claim 16 is therefore not subject to rejection under 35 U.S.C. §103(a) as unpatentalbe over Sekigawa et al. in view of Nimishakavi and further in view of Lu.

The prior art made of record and not relied upon is not considered any more pertinent to applicants' disclosure than that already cited.

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For all the foregoing reasons, applicants respectfully solicit allowance of claims 15-21 in addition to previously allowed claims 22-24.

Respectfully submitted,

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Enclosure: Abstract

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